

breakdown voltage then is 40V along with the current discharge, meeting the specific requirements for circuit protection.

[0047] While the principles of the invention have been described herein, it is to be understood by those skilled in the art that this description is made only by way of example and not as a limitation as to the scope of the invention. Other embodiments are contemplated within the scope of the present invention in addition to the exemplary embodiments shown and described herein. Modifications and substitutions by one of ordinary skill in the art are considered to be within the scope of the present invention, which is not to be limited except by the following claims.

What is claimed is:

1. A monolithically-integrated dual surge protective device, comprising a LDMOS device, and a diode assembly which comprises multiple diodes series-wound on back to back basis in the following sequence:

N-P-...-N-P-N-P-N-...-P-N-;

wherein one end of the diode assembly is connected to a drain electrode of the LDMOS device and the other end is connected to a gate electrode of the LDMOS device.

2. The monolithically-integrated dual surge protective device of claim 1, wherein the diode assembly is fabricated and formed on a polysilicon thin film by means of ion injection technique.

3. The monolithically-integrated dual surge protective device of claim 2, wherein the diode assembly is fabricated on the gate oxide layer between the drain electrode and gate electrode of the LDMOS device.

4. The monolithically-integrated dual surge protective device of claim 3, wherein the width-to-length ratio of the channel of the LDMOS device is 10 or more.

5. The monolithically-integrated dual surge protective device of claim 4, wherein the length and width of the channel of the LDMOS device are 5 and 50 microns, respectively.

6. A combination of two or more dual surge protective devices connected in parallel, each device being made in accordance with claim 1.

7. A method of fabricating the monolithically-integrated dual surge protective device of claim 1, wherein the diode assembly is fabricated in the gate electrode area of the LDMOS device after fabrication of the LDMOS device is completed, comprising the steps of:

- a) depositing a polysilicon layer having a thickness of 0.5 to 3 microns on a gate oxide layer of the LDMOS device using chemical vapor deposition and mixing P-type dopant to form P-type polysilicon during the deposition;
- b) using photo-etching to define N-type regions on the polysilicon and using ion injection to inject N-type dopant to form the N-type regions in a section;
- c) depositing a passivation layer above said polysilicon layer; and
- d) connecting a first end of the diode directly to the gate electrode and a second end of the diode directly to the drain electrode of the LDMOS device during a process of metallization.

8. The method of claim 7, wherein:

- a) the P-type dopant is boron with a concentration of $10^{19}/\text{cm}^3$; and
- b) the N-type dopant is phosphorous ions with a concentration of $10^{19}/\text{cm}^3$.

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